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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,672	OKADA, KOJI	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Michael B. Shingleton

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-6, 8, 12, 14-17, 19 and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sha et al. 6,404,294 (Sha).

Figures 7, 12, 13 and 16, and the relevant text of Sha disclose a phase locked loop (pll) spread spectrum clock generator.

With respect to independent claim 1, element 202 of Sha is a phase comparator that receives a "standard clock signal" (REF) and a "operating clock signal" FOUT (Note that the output of the frequency divider 208 is directly connected to the input of the phase comparator and thus the phase comparator receives the FOUT signal in an indirect manner. Note that this is the manner as that of applicant's discloses invention. In particular note Figure 3, where the CLK signal is applied to the phase comparator 10 in an indirect manner through the frequency divider 17.) Element 100 of Sha is voltage controlled oscillator (VCO) that generates the operating clock signal FOUT based on the output signal of the phase comparator 202 as is clearly illustrated. Internal to the VCO is a voltage to current converter composed of at least element 118. Element 110' forms a current D/A converter that fluctuates the current signal based on a digital signal. Note that the digital signal selects the gain and thus as shown in Figure 13 for a different VIN a different FOUT will be obtained. In other words the current input to the current controlled oscillator element 114 will change in accordance with the change in the digital signal. In the In re Schreiber, 128 F.3d 1473, 1478 44 USPQ2d 1429, 1432 (Fed. Cir. 1997) case the court held that the prior art patent anticipated applicant's invention since "the patent would be capable of performing the functions recited in applicant's claim" (See MPEP 2112.01 V.). In the instant case this structure of Sha is fully capable of providing the function of "for spreading spectrum" because when the digital signal applied to the current D/A converter is changed in Sha this structure will provide the function of "spreading" the spectrum, i.e. it will cause a change in the frequency of the operating clock signal even though that change may be temporary. This change in the frequency is like that of applicant's disclosed invention. Note that for example Figure 3 of

applicant's invention when the variable current source (Note the element 110' of Sha is just a variable current source.) is changed this causes a change in the current in accordance with the difference detected by the phase comparator 10. Accordingly, there is no structural difference between the claimed invention and the structure of Sha. In addition MPEP 2114 is very specific that in a claim drawn to structure it is the structure that must distinguish the claim over the prior art. Note that the claimed of the instant invention do not recite a means that causes the digital signal to vary with a specifically claimed rate or rates. The claims are broad in this aspect.

With respect to independent claim 6, the FOUT signal is the "operating clock" signal that is generated based on the current signal produced by the "first circuit" composed of elements like 118 and 110'. The current signal is based on a result of a comparison between a "standard clock" (REF) and a "comparison clock" (The output of the feedback divider 208) via the phase detector 202. Element 118 of the first circuit will produce a plurality of current signals. Furthermore element 110' of the first circuit produces a plurality of current signals. The second circuit is formed by element 114 of Sha and this element is the actual element that produces a plurality of operating clock signals FOUT whose frequencies are different with each other based on the plurality of the current signals. Element 110' is a current D/A converter that is controlled by a digital signal VCTRL[n:1].

With respect to independent claim 12, the first clock generator part is composed of at least the phase comparator 202 and a voltage to current converter 118. The phase comparator 202 compares a standard clock signal (REF) and an operating clock signal (FOUT) indirectly via the output of the frequency divider 208. (Note that the same thing occurs in Applicant's disclosed invention and in particular note Figure 6 of the instant application.) Element 114 (first current controlled oscillator.) is also part of the first clock generator wherein the "first clock signal" (FOUT) is based on the current at the input of this device. The second clock generator of Sha is formed by the current D/A converter 110' that converts a digital signal into a current signal. This current signal is combined with the current signal of the voltage to current converter to thereby form a second clock signal. Element 114 also forms a second current controlled oscillator for the second clock generator. Note that the digital signal selects the gain and thus as shown in Figure 13 for a different VIN a different FOUT will be obtained. In other words the current input to the current controlled oscillator element 114 will change in accordance with the change in the digital signal. In the In re Schreiber, 128 F.3d 1473, 1478 44 USPQ2d 1429, 1432 (Fed. Cir. 1997) case the court held that the prior art patent anticipated applicant's invention since "the patent would be

capable of performing the functions recited in applicant's claim" (See MPEP 2112.01 V.). In the instant case this structure of Sha is fully capable of providing the function of "for spreading spectrum" because when the digital signal applied to the current D/A converter is changed in Sha this structure will provide the function of "spreading" the spectrum, i.e. it will cause a change in the frequency of the operating clock signal even though that change may be temporary. This change in the frequency is like that of applicant's disclosed invention. Note that for example Figure 3 of applicant's invention when the variable current source (Note the element 110' of Sha is just a variable current source.) is changed this causes a change in the current in accordance with the difference detected by the phase comparator 10. Accordingly, there is no structural difference between the claimed invention and the structure of Sha. In addition MPEP 2114 is very specific that in a claim drawn to structure it is the structure that must distinguish the claim over the prior art. Note that the claimed of the instant invention do not recite a means that causes the digital signal to vary with a specifically claimed rate or rates. The claims are broad in this aspect.

With respect to claim 17, the first circuit is formed by the phase locked loop (pll) that is formed by at least the phase comparator 202, the charge pump the filter 206, the voltage to current converter 118 and the current controlled oscillator 114. Going back to applicant's specification this is the same basic pll structure like Figure 1 and Figure 3 that forms the single peak spectrum shown in Figures 2 and Figure 5 of the disclosed invention. Thus the first clock signal of Sha is a frequency spectrum containing N number of peaks. The second circuit of claim 17 is met by the current D/A converter. Here as noted above the digital signal VCTRL[n:1] changes the current and gain and thus the frequency is changed when the VCTRL[n:1] signal is changed or varied. This changing of the current even for a short period of time i.e. the time it takes for the feedback loop of the pll to readjust the frequency output causes a spreading of the spectrum. Thus there are three bits in the digital signal and thus there is the possibility of eight changes in the gain and hence the frequency output resulting in at least eight number of peaks one for each value of the digital signal. Thus M in Sha is greater than N. The phase comparator 202 of Sha causes the comparison of the standard clock REF from the operating clock that is indirectly applied to the phase comparator 202 via the frequency divider 208. Note that the digital signal selects the gain and thus as shown in Figure 13 for a different VIN a different FOUT will be obtained. In other words the current input to the current controlled oscillator element 114 will change in accordance with the change in the digital signal. In the In re Schreiber, 128 F.3d 1473, 1478 44 USPQ2d 1429, 1432 (Fed. Cir. 1997) case the court held that the prior art patent anticipated applicant's invention since "the patent would be capable of performing the functions

recited in applicant's claim" (See MPEP 2112.01 V.). In the instant case this structure of Sha is fully capable of providing the function of "for spreading spectrum" because when the digital signal applied to the current D/A converter is changed in Sha this structure will provide the function of "spreading" the spectrum, i.e. it will cause a change in the frequency of the operating clock signal even though that change may be temporary. This change in the frequency is like that of applicant's disclosed invention. Note that for example Figure 3 of applicant's invention when the variable current source (Note the element 110' of Sha is just a variable current source.) is changed this causes a change in the current in accordance with the difference detected by the phase comparator 10. Accordingly, there is no structural difference between the claimed invention and the structure of Sha. In addition MPEP 2114 is very specific that in a claim drawn to structure it is the structure that must distinguish the claim over the prior art. Note that the claimed of the instant invention do not recite a means that causes the digital signal to vary with a specifically claimed rate or rates. The claims are broad in this aspect.

With respect to claim 19, element 202 forms a phase comparator that compares a standard clock signal REF and an operating clock signal (FOUT) indirectly via the output of the frequency divider 208. (Note the same thing occurs in Applicant's disclosed invention and in particular note Figure 6 of the instant application.) Element 204 is a charge pump whose output is based upon the comparison preformed by the phase comparator. Element 100 is the voltage controlled oscillator (VCO) that outputs the operating clock signal (FOUT) based on the output of the charge pump. The VCO includes a voltage to current converter 118 that converts the voltage signal form the charge pump to a current signal. The element 110' forms a current D/A converter that changes the current signal into a variable current signal based upon the digital signal VCTRL[n:1]. Element 114 form a current controlled oscillator that oscillates the operating clock signal based on the variable current signal. Note that the digital signal selects the gain and thus as shown in Figure 13 for a different VIN a different FOUT will be obtained. In other words the current input to the current controlled oscillator element 114 will change in accordance with the change in the digital signal. In the In re Schreiber, 128 F.3d 1473, 1478 44 USPQ2d 1429, 1432 (Fed. Cir. 1997) case the court held that the prior art patent anticipated applicant's invention since "the patent would be capable of performing the functions recited in applicant's claim" (See MPEP 2112.01 V.). In the instant case this structure of Sha is fully capable of providing the function of "for spreading spectrum" because when the digital signal applied to the current D/A converter is changed in Sha this structure will provide the function of "spreading" the spectrum, i.e. it will cause a change in the frequency of the operating clock signal even though that change

may be temporary. This change in the frequency is like that of applicant's disclosed invention. Note that for example Figure 3 of applicant's invention when the variable current source (Note the element 110' of Sha is just a variable current source.) is changed this causes a change in the current in accordance with the difference detected by the phase comparator 10. Accordingly, there is no structural difference between the claimed invention and the structure of Sha. In addition MPEP 2114 is very specific that in a claim drawn to structure it is the structure that must distinguish the claim over the prior art. Note that the claimed of the instant invention do not recite a means that causes the digital signal to vary with a specifically claimed rate or rates. The claims are broad in this aspect.

With respect to claim 20, here a method for clock generation is recited. The structure as indicated above provides for the claimed method steps. This includes the step of comparing a standard clock signal REF with an operating clock signal (FOUT) in an indirect manner through the frequency divider 208. The step of converting the results of the comparison step to a current signal is preformed by the element 118. The step of using a D/A converter to change the current signal into variable current signals based on the digital control signal for spreading spectrum is preformed by the current D/A converter 110' and the means that produces the control signal VCTRL[n:1]. Note that when the VCTRL[n:1] is changed this causes a change in the current and hence a change in the frequency as clearly illustrated in Figure 13 of Sha. Sha is clear that the VCTR[n:1] signal is varied, but is silent on the way it is varied. For example Sha does not state that the control signal VCTRL[n:1] is continually varied in a random manner at a particular rate. The claims only recite that the current is varied and is not specific on the period at which the current is varied. Thus Sha clearly will meet this method step of varying the current. The operating clock signal produced by Sha will accordingly vary in frequency based on the variable current signal.

The clock signal FOUT that is outputted will then occur with varying frequencies based on the variable current signal from the element 118 and the current D/A converter.

With respect to dependent claims like claim 4, here a control circuit is recited as controlling the current D/A converter. There must be a control circuit in Sha that produces the VCTRL[n:1] signal. This electrical signal cannot just occur without there being a circuit to produce it.

With respect to dependent claims like claim 5, here a "determining circuit" is recited that have the function of to determine the range of change of frequency of the clock oscillated by the current controlled oscillator. As recited above the range of the VCTRL[n:1] signal in controlling

the gain will control the range of change of frequency as is clearly illustrated by Figure 13 of Sha.

With respect to dependent claims like claim 8, it goes without saying that the first circuit "118 ad 110'" has a control circuit that includes elements like the phase comparator that controls the first circuit as is clearly shown (See Figure 16 of Sha.).

With respect to dependent claims like claim 16, it goes with say that the first clock circuit being connected to the phase comparator forms a "corrective circuit". Note the feedback in the Figure 16 arrangement of Sha.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 7, 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha et al. 6,404,294 (Sha) in view of Applicant's Admitted prior art as represented by Figure 1(AAPA).

The reasoning involving Sha as it relates to the rejection of claims 1, 4-6, 8, 12, 14-17, 19 and 20 and the following. Claims like claim 2 recites a frequency divider dividing the operation clock signal. This corresponds to elements like 55 shown in the disclosed invention. As mentioned above element 208 of Sha is a frequency divider and as such this structure meets the frequency divider dividing the operation clock signal. Claim 2 also recites a first frequency dividing circuit frequency-dividing the standard clock signal. The practice of employing a frequency divider after the reference clock generator in a phase locked loop (pll) is a common practice. This clearly allows for a higher frequency clock to be used and also allows for the signal applied to the phase comparator of the phase locked loop to be varied or changed by the selection of the division factor of the frequency divider which results in greater control of the frequency of the pll.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized/provide a frequency divider between the reference clock

(REF) and the phase comparator 202 in Sha so as to allow for a higher frequency reference clock generator to be used and to allow for the signal at the "REF" input terminal of the phase comparator 202 to be changed so as to allow for greater control of the frequency of the pll as taught by AAPA.

With respect to claims like claims 3 and 7, here claims 3 and 7 recite the use of a current D/A converter that employs a low pass filter. The examiner sees no specific drawing or description that shows or describes the specifics of the current D/A converter that employs a low pass filter. The only drawing figure the examiner can find that relates to a current D/A converter that employs a low pass filter is the black box diagram 81 shown in Figure 22 of the disclosed invention. Thus since a black box has been used to signify this structure and the specification is not specific on this structure, the structure represented is seen as conventional. However, conventional current D/A converters that employ a low pass filter as part of their structure are one conventional art recognized form of current D/A converter. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the current D/A converter of Sha with one that employs a low pass filter since the examiner takes Official Notice of the equivalence of the current D/A converter that employs a low pass filter and the current D/A converter of Sha for their use in the electronic circuitry art and the selection of any of these known equivalents to provide a D/A function would be within the level of ordinary skill in the art. (Note that art recognized equivalence is a proper motivation to combine MPEP 2144.06, 2144.07 and 2144.03). The motivation here is further supported by the fact that applicant implies that the structure of element 81 is conventional and the examiner sees no statement of unexpected results that results from the use of that conventional structure.

Response to Arguments

Applicant's arguments filed 01-03-2006 have been fully considered but they are not persuasive. The examiner sees no remarks concerning the rejection of claim 6. It is also noted that claim 6 has not been amended. The main argument applicant makes relates to the newly added limitation relating to there being a digital signal that is "for spreading spectrum" added to most of the independent claims where applicant believes that such a limitation is not taught nor suggested by the prior art or record. The examiner respectfully disagrees. Specifically, note Figures 3, 6 and 21 of the instant invention. Also note pages 9 and 10 of the instant application. Here the basic pll circuit is shown. In these circuits the two frequency dividers are the elements that set the operating frequency of the pll. The variation in the current causes only a temporary

change in the output frequency of the circuit. The feedback loop in combination with the phase comparator will force the output frequency back to the level where the phase comparator "matches" the phase of the two frequency dividers like 9 and 17 of Figure 3. Sha is the same basic structure and therefore operates the same as that of applicant's invention. In Sha the REF frequency and the output of the frequency divider 208 determines the final run or output frequency of the circuit. When the digital signal VCTRL[n:1] changes, the current output to the element 114 changes causing a change in the output frequency which is like that of applicant's invention for it will be only temporary because the feedback loop will force the frequency to be such that the phase matches between the REF frequency and the output of the frequency divider. Thus applicant's argument that the digital signal of Sha cannot cause a "spreading of the spectrum" is respectfully disagreed with. Sha is fully capable of "spreading the spectrum" and the examiner contends that such occurs every time the digital signal VCTRL[n:1] is changed. Furthermore applicant has not pointed out what the structural differences are between the claimed invention and the prior art. MPEP 2114 requires that "while features of an apparatus may be recited either structurally or functionally, claim directed to an apparatus must be distinguished from the prior art in terms of structure rather than function."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
March 17, 2006

Michael B Shingleton

Primary Examiner
Group Art Unit 2817